For more information, contact:
Nanette Collins
Public Relations for SmartDV
(617) 437-1822
nanette@nvc.com

SmartDV, Aldec Partner to Link SmartDV's Verification IP with Aldec's Riviera-PRO Simulator

Will Cooperate Technically to Ensure Respective Tools Work Together, Jointly Market their Solutions

SAN JOSE, CALIF. and HENDERSON, NEV. — July 20, 2020 — SmartDV™ Technologies, the ***Proven*** and ***Trusted*** choice for Design and Verification Intellectual Property (IP), and Aldec today inked an agreement linking SmartDV's Verification IP with Aldec's Riviera-PRO™ high-performance simulation and debugging tool.

Under terms of the agreement, SmartDV and Aldec, a pioneer in mixed HDL language simulation and hardware-assisted verification for FPGA and ASIC designs, will cooperate technically to ensure their respective Verification IP and simulator work together. They agreed as well to jointly market their solutions.

"Aldec has been an EDA industry pioneer since 1984 providing verification solutions for FPGA and ASIC designers," says Deepak Kumar Tala, SmartDV's managing director. "Both are important market segments for us, making an Aldec

partnership an imperative to broaden our support for industry simulators so that SmartDV Verification IP can be used on any platform for various types of design."

"SmartDV is an industry leader for Design and Verification IP solutions offering comprehensive and up-to-date support for many standard protocols," remarks Louie De Luna, director of marketing at Aldec. "Our users will benefit from having access to SmartDV's broad portfolio of Design and Verification and we welcome the opportunity to build a long-lasting relationship."

Aldec's Riviera-PRO addresses verification needs of engineers crafting tomorrow's cutting-edge FPGA and SoC devices. The tool enables the ultimate testbench productivity, reusability, and automation by combining the high-performance simulation engine, advanced debugging capabilities at different levels of abstraction, and support for the latest Language and Verification Library Standards.

SmartDV's extensive Verification IP portfolio is compatible with all verification languages, platforms and methodologies and used throughout a coverage-driven chip design verification flow in simulation, emulation, FPGA prototyping and formal verification environments. A proprietary, automated compiler-based technology ensures quick delivery of its offerings compliant with standard protocol specifications for new or evolving applications.

SmartDV and Aldec at Virtual DAC

SmartDV and Aldec will exhibit virtually at the 57th Design Automation Conference (DAC) starting Monday, July 20, through Saturday, August 1. The Virtual Expo Hall will be open with Live Chat hours from 10:30 a.m. until 1:30 p.m. P.DT. Monday through Wednesday, July 20-22.

About SmartDV

SmartDV™ Technologies is the ***Proven*** and ***Trusted*** choice for Design and Verification IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. SmartDV offers high-quality standard protocol Design and Verification IP for simulation, emulation, field programmable gate array (FPGA) prototyping, post-silicon validation, formal property verification and RISC-V CPU verification. Any of its Design and Verification IP solutions can be rapidly customized to meet specific customer design needs. The result is ***Proven*** and ***Trusted*** Design and Verification IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif.

Connect with SmartDV at:
Website: www.Smart-DV.com
Linkedin: https://www.linkedin.com/company/smartdv-technologies/about/
Twitter: @SmartDV

About Aldec

Aldec Inc., headquartered in Henderson, Nev., is an industry leader in Electronic Design Verification and offers a patented technology suite including: RTL Design, RTL Simulators, Hardware-Assisted Verification, SoC and ASIC Prototyping, Design Rule Checking, CDC Verification, IP Cores, Requirements Lifecycle Management, DO-254 Functional Verification and Military/Aerospace solutions. www.aldec.com.