SmartDV™

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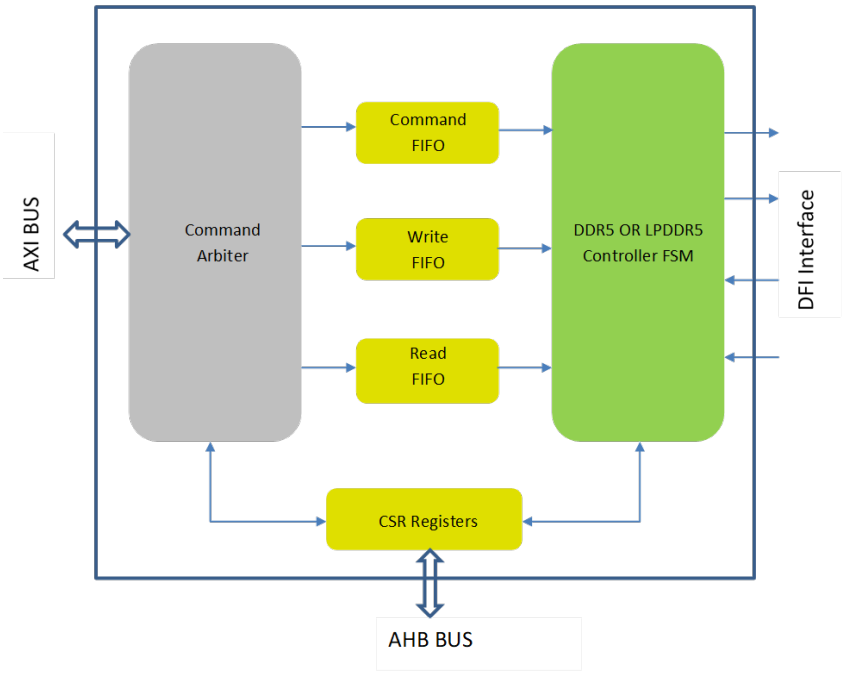
SmartDV Offers New Design IP for DDR5 and LPDDR5

Fast, New Controller Design IP Offers Low Power and Latency, Reduced Gate Count

SAN JOSE, CALIF. — February 18, 2020 — SmartDV™ Technologies, the ***Proven*** and ***Trusted*** choice for Design and Verification Intellectual Property (IP), today introduced its new Design IP for DDR5 and LPDDR5 SDRAM controllers.

The fast, efficient DDR5 and LPDDR5 Design IP offers low power and latency, reduced gate count for increased memory interface bandwidth, and fully supports the latest DDR5 and LPDDR5 specifications. The IP targets multiple applications such as high-performance computing, networking, wearables, IoT and mobile, and can be rapidly customized to meet specific user needs.

“SmartDV’s DDR5 and LPDDR5 Design IP fully supports the DDR5 and LPDDR5 specifications intended to meet higher memory bandwidth requirements and address efficient data throughput," comments Deepak Kumar Tala, SmartDV’s managing director.



Caption: SmartDV's DDR5 and LPDDR5 Design IP (in green box) offer low power and latency, reduced gate count for increased memory interface bandwidth.

SmartDV's DDR5 Controller Design IP Core supports the JESD79-5 Rev095 protocol standard specification, while its LPDDR5 Controller Design IP core supports the JESD209-5 LPDDR5 protocol standard specification. Both are compatible with DFI 5.0 and support a variety of host bust interfaces, including AHB, APB, OCP, TileLink, Wishbone, VCI and Avalon PLB. An open, flexible architecture ensures they can be used for any custom bus interface.

SmartDV will exhibit its Design and Verification IP portfolio at DVCon U.S. (Booth #304). Exhibits will be open during DVCon Expo and Reception Monday, March 2, from 5 p.m. until 7 p.m., Tuesday, March 3, and Wednesday, March 4, from 2:30 p.m. until 6 p.m. DVCon U.S. will be held at the DoubleTree Hotel in San Jose, Calif.

DVCon attendees can schedule meetings or private demonstration via email at demos@Smart-DV.com or sales@Smart-DV.com.

Availability and Pricing

The SmartDV DDR5 and LPDDR5 Design IP is delivered as soft design IP with register transfer level (RTL) source code and a comprehensive test suite that can be implemented in ASIC, SoC or FPGA designs. They are available today.

Pricing is available upon request.

Email requests for datasheets or more information should be sent to sales@Smart-DV.com

About SmartDV

SmartDV™ Technologies is the ***Proven*** and ***Trusted*** choice for Verification and Design IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. Its high-quality standard protocol Design and Verification IP for simulation, emulation, field programmable gate array (FPGA) prototyping, post-silicon validation, formal property verification and RISC-V CPU verification. Any of its Design and Verification IP solutions can be rapidly customized to meet specific customer design needs. The result is ***Proven*** and ***Trusted*** Design and Verification IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif.

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