MEDIA ALERT

SmartDV™

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SmartDV to Feature Smart ViPDebug, Extensive Portfolio of Verification, Design, Assertion, Post-Silicon IP, Synthesizable Transactors at ES Design West

Will Present "Design Successes with Verification IP" as part of the ES Design West "Meet the Experts" Program

SAN JOSE, CALIF — June 27, 2019 —

WHO: SmartDV™ Technologies, the ***Proven*** and ***Trusted*** choice for Verification Intellectual Property (VIP) supporting simulation emulation, field programmable gate array (FPGA), formal models and post-silicon validation platforms, Design IP and rapid customized VIP and Design IP development

WHAT: Will demonstrate Smart ViPDebug™, a protocol debugger that rapidly identifies violations through linked waveform and transaction database views to reduce debug time in booth #2226 at ES Design West, a co-located event at SEMICON West. Highlighted will be SmartDV's comprehensive portfolio of VIP compatible with all verification languages, platforms and methodologies, Design IP, SimXL™ portfolio of Synthesizable Transactors, assertion IP and post-silicon VIP. Featured VIP will be its

new OpenCAPI, Compute Express Link (CXL), Ethernet Time-Sensitive Networking (TSN) and TileLink interconnect standards.

WHEN: Tuesday through Thursday, July 9-11. ES Design West attendees can schedule demonstrations through: demo@smart-dv.com

WHERE: Moscone Center South Hall in San Francisco

Bipul Talukdar, SmartDV's director of Applications Engineering North America, will present "Design Successes with Verification IP" as part of the ES Design West "Meet the Experts" Advanced Applications session Thursday, July 11, at 3:10pm. It will be held at the SMART Design Pavilion.

About SmartDV

SmartDV™ Technologies is the ***Proven*** and ***Trusted*** choice for Verification and Design IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. Its high-quality standard or custom protocol Verification and Design IP are compatible with all verification languages, platforms and methodologies supporting all simulation, emulation and formal verification tools used in a coverage-driven chip design verification flow. The result is ***Proven*** and ***Trusted*** Verification and Design IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif. Visit SmartDV to learn more.

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