SmartDV™

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SmartDV Announces Availability of Ethernet TSN Design IP
Fully Compliant with Updated IEEE Standard for Time-Sensitive Transmission of Data over Ethernet Networks

SAN JOSE, CALIF — September 17, 2019 — SmartDV™ Technologies, the ***Proven*** and ***Trusted*** choice for Design and Verification Intellectual Property (IP), today announced its Design IP for the Ethernet Time-Sensitive Networking (TSN) protocol, an update to the IEEE standard for time-sensitive transmission of data over Ethernet networks.

"The traditional Ethernet protocol was designed to deliver data reliably but not to a specific time standard," remarks Deepak Kumar Tala, managing director of SmartDV. For safety and performance reasons, many new applications including autonomous driving systems demand timely, reliable data. The more rigorous Ethernet TSN protocol specification requires that all devices be time-synchronized and deterministic to ensure data is not lost or delayed. Our development group, many of whom designed Ethernet products at leading network architecture companies, took on the challenge, leveraging our proprietary automated Smart Compiler."

SmartDV's Ethernet TSN Design IP, a full-featured, easy-to-use, synthesizable design that supports various Ethernet TSN standards and 10-, 100- and 1,000-megabit speeds, is fully compliant with IEEE 802.1 specifications defining various components of time-sensitive networking.

The IP, tested on a field programmable gate array (FPGA) platform and validated with SmartDV's Verification IP used to tape out ASIC designs, includes advanced configuration and status reporting interface.

In addition to Ethernet TSN, SmartDV offers a range of Ethernet Design IP to support 10, 100, 1G, 10G, 40G, 100G, 200G and 400G Ethernet. All are IEEE 802.3 compliant.

Pricing and Availability

The SmartDV Ethernet TSN Design IP is shipping now.

Pricing is available upon request.

About SmartDV

SmartDV™ Technologies is the ***Proven*** and ***Trusted*** choice for Verification and Design IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. Its high-quality standard or custom protocol Design and Verification IP are compatible with all verification languages, platforms and methodologies supporting all simulation, emulation, field programmable gate array (FPGA) prototyping and formal verification tools used in a coverage-driven chip design verification flow. The result is ***Proven*** and ***Trusted*** Design and Verification IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore,

India, with U.S. headquarters in San Jose, Calif. Visit SmartDV to learn more.

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