MEDIA ALERT

SmartDV™

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SmartDV to Demonstrate New Smart ViPDebug Protocol Debugger at DAC
Latest Verification IP Solutions for TileLink, CXL, Ethernet TSN Also Featured

SAN JOSE, CALIF — May 29, 2019 —

WHO: SmartDV™ Technologies, the ***Proven*** and ***Trusted*** choice for Verification Intellectual Property (VIP), emulation, field programmable gate array (FPGA), formal models and post silicon validation platforms, Design IP and rapid customized VIP and Design IP development

WHAT: Will demonstrate its new Smart ViPDebug™, a protocol debugger that rapidly identifies violations through linked waveform and transaction database views to reduce debug time at Design Automation Conference (DAC) in booth #514. Also featured will be its latest VIP Solutions to support TileLink, Compute Express Link (CXL) and Ethernet Time-Sensitive Networking (TSN) interconnect standards. Its extensive portfolio of VIP compatible with all verification languages, platforms and methodologies will be highlighted as well.

WHEN: Monday-Wednesday, June 3-5, from 10 a.m. until 6 p.m. DAC attendees can schedule demonstrations through SmartDV's online scheduler.

WHERE: Las Vegas Convention Center in Las Vegas, Nev.

SmartDV is the first VIP Solutions provider to support TileLink, CXL and Ethernet TSN interconnect standards. The TileLink chip-scale interconnect standard is an open-source, high-performance and scalable cache-coherent fabric for RISC-V based system on chip (SoC) designs

CXL is a new high-speed CPU-to-device and CPU-to-memory interconnect to accelerate the performance of next-generation data centers. The technology is based on the PCI Express® (PCIe®) infrastructure.

Ethernet TSN is an update to the IEEE standard for time-sensitive transmission of data over Ethernet networks. SmartDV's Ethernet TSN is fully compliant with IEEE 802.1 specifications that define various components of time-sensitive networking.

About SmartDV

SmartDV™ Technologies is the ***Proven*** and ***Trusted*** choice for Verification and Design IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. Its high-quality standard or custom protocol Verification and Design IP are compatible with all verification languages, platforms and methodologies supporting all simulation, emulation and formal verification tools used in a coverage-driven chip design verification flow. The result is ***Proven*** and ***Trusted*** Verification and Design IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is

headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif. Visit

SmartDV to learn more.

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