SmartDV™

For more information, contact:
Nanette Collins
Public Relations for SmartDV
(617) 437-1822
nanette@nvc.com

SmartDV Delivers First-to-Market MIPI A-PHY v1.0 Verification IP
Firmly Establishes SmartDV, its Proven and Trusted Verification IP in the Automotive Market Segment

SAN JOSE, CALIF. –– September 22, 2020 –– SmartDV™ Technologies once again is the first company to ship Verification intellectual property (IP) to support MIPI A-PHY v1.0, the industry-standard, long-reach serializer-deserializer (SerDes) physical layer interface, delivering it as the MIPI Alliance announced availability.

MIPI A-PHY v1.0's asymmetric long-reach physical layer interface forms the cornerstone of the MIPI Automotive SerDes Solutions (MASS) that provide connectivity for Advanced driver-assistance systems (ADAS), in-vehicle infotainment (IVI) and other surround-sensor applications. "Our swift response and immediate availability of our MIPI A-PHY v1.0 Verification IP firmly establishes us in the automotive market segment," affirms Deepak Kumar Tala, managing director of SmartDV, the ***Proven*** and ***Trusted*** choice for Design and Verification IP. "This achievement is due to our proprietary, automated compiler-based technology that ensures our IP is compliant with standard protocol specifications for new or evolving applications."

As with all SmartDV fast, highly configurable and reusable plug-and-play Verification IP, users get to market quickly and confidently. The MIPI A-PHY v1.0 Verification IP can be used throughout a coverage-driven chip design verification flow in simulation, emulation, field programmable gate array (FPGA) prototyping. It also features SimXL™, Synthesizable Transactors for accelerating system-level, system-on-chip (SoC) testing on hardware emulators or FPGA prototyping platforms. SimXL allows early software development on an FPGA platform, as well as fast porting of simulation tests to emulators and FPGA platforms.

A configurable bus functional model (BFM), protocol monitor and library of integrated protocol checks come standard with SmartDV's Verification IP. The IP supports all major verification languages and methodologies, including the open verification methodology (OVM), universal verification methodology (UVM) and SystemC.

Availability and Pricing

The SmartDV MIPI A-PHY v1.0 Verification IP is available now and backed by an experienced R&D team that works individually with each user installation. Advanced configuration and status reporting interfaces are supplied, along with a comprehensive test suite that can be implemented in ASIC, SoC or FPGA designs.

Pricing is available upon request. Fast turnaround customization is available.

Email requests for datasheets or more information should be sent to sales@Smart-DV.com.

About SmartDV

SmartDV™ Technologies is the ***Proven*** and ***Trusted*** choice for Design and Verification IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. SmartDV offers high-quality standard protocol Design and Verification IP for simulation, emulation, field programmable gate array (FPGA) prototyping, post-silicon validation, formal property verification and RISC-V CPU verification. All of its Design and Verification IP solutions can be rapidly customized to meet specific customer design needs. The result is ***Proven*** and ***Trusted*** Design and Verification IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif.

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