SmartDV™

For more information, contact:
Nanette Collins
Public Relations for SmartDV
(617) 437-1822
nanette@nvc.com

SmartDV Ships First Design and Verification IP for MIPI RFFE v3.0 Specification
Users Take Delivery on New SmartDV IP as MIPI Alliance Unveils Latest Specification

SAN JOSE, CALIF. — May 12, 2020 — SmartDV™ Technologies is the first vendor to deliver Design and Verification intellectual property (IP) supporting the MIPI RF Front End Control Interface (MIPI RFFE) v3.0 specification, shipping it as the MIPI Alliance announced availability.

The SmartDV MIPI RFFE v3.0 protocol portfolio of Design and Verification IP includes simulation IP, assertion IP, post-silicon validation IP and SystemC models, along with RFFE master and slave Design IP. Also part of the portfolio is SimXL™, Synthesizable Transactors for accelerating system-level, system-on-chip (SoC) testing on hardware emulators or field programmable gate array (FPGA) prototyping platforms. In addition to fast porting of simulation tests to emulators and FPGA platforms, SimXL enables early software development on an FPGA platform.

“The new MIPI RFFE 3.0 specification will enable the advance of 5G, a growth opportunity our user community is following quite closely," says Deepak Kumar Tala,

SmartDV's managing director. "It is critical to us to quickly deliver high-quality Design and Verification IP to meet our users' exacting needs that match the features and benefits of MIPI RFFE v3.0. That's why SmartDV continues to be the ***Proven*** and ***Trusted*** IP vendor."

A de facto standard interface for control of radio frequency (RF) front-end (FE) subsystems, the new MIPI RFFE v3.0 protocol is designed for tight timing precision and low latencies needed to support 5G. It includes a two-wire interface to control RF subsystems for amplifiers, tuners, switches and filters and enhanced triggering and functionality including timed, mappable and extended triggers.

Availability and Pricing

The entire SmartDV MIPI RFFE v3.0 protocol portfolio is available now. As with all SmartDV's Design and Verification IP, its new MIPI RFFE v3.0 protocol Design and Verification IP enables users to get to market quickly and confidently. They are fast, highly configurable and reusable plug-and-play Design and Verification IP solutions for supporting the demanding needs and precision for 5G and other RF applications.

Fast turnaround customization is available.

Pricing is available upon request.

Email requests for datasheets or more information should be sent to sales@Smart-DV.com.

About SmartDV

SmartDV™ Technologies is the ***Proven*** and ***Trusted*** choice for Verification and Design IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. Its high-quality standard protocol Design and

Verification IP for simulation, emulation, field programmable gate array (FPGA) prototyping, post-silicon validation, formal property verification, RISC-V verification services can be rapidly customized to meet specific customer design needs. The result is ***Proven*** and ***Trusted*** Design and Verification IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif.

Connect with SmartDV at:
Website: www.Smart-DV.com
Linkedin: https://www.linkedin.com/company/smartdv-technologies/about/
Twitter: @SmartDV