SmartDV™

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SmartDV's Design and Verification Solutions Portfolio Surpasses 600 Offerings

Products Include Design and Verification IP, Formal Verification IP, Post-Silicon Verification IP, Synthesizable Transactors

SAN JOSE, CALIF. — June 9, 2020 — SmartDV™ Technologies, the ***Proven*** and ***Trusted*** choice for Design and Verification Intellectual Property (IP), reached a milestone in May with availability of more than 600 Design and Verification solutions.

Products range from Design and Verification IP, Formal (assertion) Verification IP, Post-Silicon Verification IP to SimXL™, a portfolio of synthesizable transactors for accelerating system-level, system-on-chip (SoC) testing on hardware emulators or field programmable gate array (FPGA) prototyping platforms.

SmartDV's proprietary, automated compiler-based technology ensures quick delivery of its product offerings compliant with standard protocol specifications for new or evolving networking, storage, automotive, bus, MIPI, display and defense and aerospace applications. As a result, SmartDV often supplies first-to-market Design and Verification solutions simultaneous to a new industry protocol standard's availability.

“Reaching 600 Design and Verification solutions is an achievement that gives all of us great satisfaction,” notes Deepak Kumar Tala, SmartDV’s managing director. “Credit goes to our experienced and tireless development group, our active participation in standards organizations and our proprietary compiler. Together, they give us a competitive advantage to quickly produce and market a host of products to support the chip design and verification process."

SmartDV’s Design and Verification solutions enable users to get to market quickly and confidently. Design IP are highly configurable and reusable plug-and-play design solutions delivered in readable register transfer level (RTL) form, lint-proof and optimized for low power, minimum area/gate count, performance and uniform quality.

Its standard and custom Verification IP enables users to verify and debug their designs quickly, easily and more effectively in simulation, emulation, FPGA prototyping, and formal verification environments used in a coverage-driven chip design verification flow.

SimXL enables early software development on FPGAs, in addition to fast porting of software simulations tests to emulators and FPGA-based prototyping platforms

Availability and Pricing

The complete portfolio of SmartDV Design and Verification solutions, backed by experienced engineers who work individually with each user installation, are available now. Custom protocol or modifications based on specific customer requests can be rapidly developed, validated and delivered.

Pricing is available upon request.

Email requests for datasheets or more information should be sent to sales@Smart-DV.com.

About SmartDV

SmartDV™ Technologies is the ***Proven*** and ***Trusted*** choice for Verification and Design IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. SmartDV offers high-quality standard protocol Design and Verification IP for simulation, emulation, field programmable gate array (FPGA) prototyping, post-silicon validation, formal property verification and RISC-V CPU verification. Any of its Design and Verification IP solutions can be rapidly customized to meet specific customer design needs. The result is ***Proven*** and ***Trusted*** Design and Verification IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif.

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