

# **NEWS RELEASE**



For more information, contact:

Nanette Collins

Public Relations for [SmartDV](#)

(617) 437-1822

[nanette@nvc.com](mailto:nanette@nvc.com)

## **SmartDV Announces Reusable Plug-and-Play Validation Solution to Test Prototype Silicon**

*Post-Silicon Verification IP Offers Efficient, High-Performance Platform*

**SAN JOSE, CALIF. — October 14, 2021 —** [SmartDV™ Technologies](#), the leader in Design and Verification Intellectual Property (IP), today announced its post-silicon verification IP (PSVIP), a reusable plug-and-play validation solution to test prototype silicon.

The PSVIP solution offers an efficient and high-performance platform for validating standard interface protocols such as those available from the MIPI Alliance. Used across projects, it is an alternative to one-off custom-built post-silicon validation platforms often needed at the end of a design project. PSVIP is used to validate either a prototype silicon device or an FPGA platform programmed with the final design. It offers the final opportunity to validate the silicon prototype device before release to volume production.

“Verification is one of the most critical and complex activities of SoC or ASIC design and acts as the gatekeeper at each stage of the process,” affirms Deepak Kumar Tala, SmartDV’s managing director. “Prior to volume production, verification engineers often employ a custom onetime use platform for testing the prototype silicon. Instead, our PSVIP offers a reusable plug-and-play alternative for verification and validation of standard interface protocols.”

SmartDV’s PSVIP solutions run on an FPGA that interfaces with the device under test (DUT) that can either be a prototype silicon device or another FPGA programmed as the DUT. The latter approach often is used prior to silicon prototypes as a final check before committing to first silicon. The solution includes a Perl driver that runs on a standard Linux or Windows host that communicates directly with the PSVIP instantiated in an FPGA. The PSVIP solution is offered as a Synthesizable RTL model or as a pre-programmed FPGA board with the PSVIP already built in. It comes with advanced configurations, error injection and a status reporting interface.

### **Availability and Pricing**

SmartDV PSVIP solutions are available now.

Pricing is available upon request.

SmartDV offers a broad portfolio of PSVIP solutions for different protocols. A proprietary in-house compiler supports rapid generation and customization of PSVIP to support specific customer needs.

Email requests for more information or the PSVIP whitepaper should be sent to [sales@Smart-DV.com](mailto:sales@Smart-DV.com).

### **About SmartDV**

[SmartDV™ Technologies](#) offers the largest portfolio of Design and Verification Intellectual Property (IP) used by more than 200 customers worldwide, including seven of the top 10 semiconductor companies and four of the largest consumer electronics companies. It supports market segments and protocols as diverse as mobile and 5G, networking and SoC, automotive and serial bus, storage, video and defense and aerospace. With more than 800 products in its portfolio, SmartDV covers the design flow with Design IP and Verification IP for use in simulation, emulation, formal and post-silicon validation and memory modeling. SmartDV has the best customer service with more than 250 experienced ASIC and SoC design and verification engineers, a global footprint and local sales offices. Its technical support is available 24 hours a day seven days a week. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif.

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