SmartDV™

For more information, contact:
Nanette Collins
Public Relations for SmartDV
(617) 437-1822
nanette@nvc.com

SmartDV's Platform-Independent VIP Portfolio Ensures Seamless Coverage-Driven Verification Flow

Broad Portfolio of Reusable Plug and Play VIP Fills Verification Coverage Gaps, Supports Code Coverage, Functional Coverage

SAN JOSE, CALIF. — November 21, 2019 — SmartDV™ Technologies, the ***Proven*** and ***Trusted*** choice for Verification Intellectual Property (VIP), today announced its broad portfolio of portable, platform-independent VIP ensures a thorough and seamless coverage-driven verification flow with no coverage gaps between simulation, emulation or formal verification.

Unlike other VIP tailored to specific verification functions, SmartDV's VIP addresses verification from simulation and formal verification to hardware emulation and post-silicon verification with support for both code coverage and functional coverage, the basis of a coverage-driven verification flow. A unique feature of the VIP is the ability to assimilate formal verification coverage into simulation coverage.

"Like design, verification is a dynamic process that requires complete coverage and a well-integrated flow with a mix of verification methodologies," comments Deepak Kumar Tala, chairman of SmartDV. "Users want thoroughness and efficiency in their

coverage-driven verification flow and do not want VIP that supports one given protocol and not others."

SmartDV fills the verification coverage gaps with a broad portfolio of VIP offerings that support code coverage and functional coverage. Using SmartDV VIP, proper code coverage executes 100% of design code during simulation with appropriate and enough stimulus scenarios. Functional coverage verifies the functionality of a design using cover properties and covergroup implemented in protocol monitors, a component of SmartDV's VIP.

Both fill a coverage metrics table offered by simulation flows from different vendors and provide different flavors of code coverage numbers and functional coverage numbers. In some cases, users of SmartDV's VIP reach 99% of their coverage metrics.

Reusable plug-and-play for standard interface protocols, the VIP is based on hardware verification languages and includes full API compatibility to move designs seamlessly from simulation through emulation. All are supported by the Smart ViPDebug™ visual debugger and offer fast compile and system-level simulation run times. Additional support includes stimulus generators, monitors, scoreboards/checkers and functional coverage models.

A proprietary, automated compiler-based technology gives SmartDV the ability to cover the entire verification flow with rapidly developed and deployed VIP, and support new or evolving standards.

Pricing and Availability

The SmartDV VIP portfolio is configurable and customizable.

Pricing is available upon request.

Email requests should be sent to demo@Smart-DV.com

About SmartDV

SmartDV™ Technologies is the ***Proven*** and ***Trusted*** choice for Verification and Design IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. Its high-quality standard or custom protocol Design and Verification IP supports simulation, emulation, field programmable gate array (FPGA) prototyping, post-silicon validation, formal property verification, RISC-V verification services. The result is ***Proven*** and ***Trusted*** Design and Verification IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif. Visit SmartDV to learn more.

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