SmartDV™

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SmartDV Adds Support for Verilator Open Source HDL Verilog Simulator
Available for All SmartDV Verification IP

SAN JOSE, CALIF. — October 1, 2019 — SmartDV™ Technologies today announced support for Verilator, the free, open-source hardware description language (HDL) simulator, becoming the first Verification Intellectual Property (VIP) provider to do so.

"An open-source simulator such as Verilator is a great option for startups or small companies with modest budgets," says Deepak Kumar Tala, managing director of SmartDV. "While it may not have the rich feature set of a commercial Verilog simulator, it offers a straightforward path to migrate synthesizable SystemVerilog to C++ or SystemC, and users are requesting support for it."

Verilator compiles synthesizable SystemVerilog and synthesis assertions into single- or multithreaded C++ or SystemC code. Designed for large projects with fast simulation performance requirements, it is used to generate executable models of CPUs for embedded software development group and simulates large multi-million gate designs with thousands of modules.

Smart DV's sizable portfolio of standard and custom protocol VIP is fully compliant with standard protocol specifications and enables users to verify and debug their designs quickly, easily and more effectively. Its networking, storage, automotive, bus, MIPI and display protocol VIP supports simulation, emulation, formal verification environments and verification languages used in a coverage-driven chip design verification flow.

Configurable and reusable, each includes SystemVerilog, Verilog, VHDL and SystemC testbench support for faster testbench development, more complete verification with built-in coverage and simplified results analysis. An easy-to-use command interface simplifies testbench control and master/slave configurations.

Features include support for uncached lightweight and heavy weight and cached conformance levels, as well as cache-coherent shared memory and FIFO memory and constrained randomization of protocol attributes. The VIP injects errors during data transfer and configure the width of all signals. A rich set of configuration parameters control functionality. With on-the-fly protocol and data checking, it notifies the testbench of significant events — transactions, warnings, timing and protocol violations, for example.

The VIP comes with a complete test suite to test every feature of the specification. Additional support features include separate address/control and data phases, and the ability to issue multiple outstanding transactions, out-of-order transaction completion, burst transfers, atomic operation and hint operation. A rich set of configuration parameters controls functionality.

SmartDV will exhibit at Arm TechCon (Booth #1132) Wednesday, October 9, from 11:30 a.m. until 6:30 p.m. and Thursday, October 10, from 11:30 a.m. until 6 p.m. at the San Jose Convention Center, San Jose, Calif. Attendees can arrange meetings to discuss its support for Verilator through demo@smart-dv.com.

Pricing and Availability

Verilator support for all SmartDV Verification IP is available now.

Pricing is available upon request.

About SmartDV

SmartDV™ Technologies is the ***Proven*** and ***Trusted*** choice for Verification and Design IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. Its high-quality standard or custom protocol Design and Verification IP are compatible with all verification languages, platforms and methodologies supporting all simulation, emulation, field programmable gate array (FPGA) prototyping and formal verification tools used in a coverage-driven chip design verification flow. The result is ***Proven*** and ***Trusted*** Design and Verification IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif. Visit SmartDV to learn more.

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